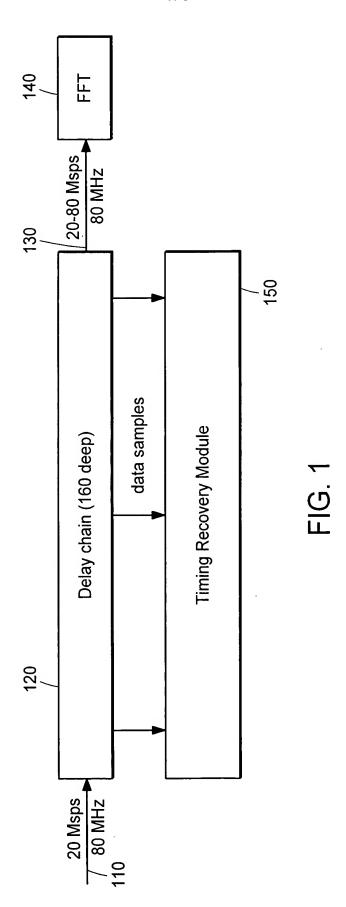Appl'n No.: 10/731,730
Title: "Method and System For Dynamically..."
Inventors: Maneesh Soni, *et al.*
Replacement Sheet

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FIG. 1

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FIG. 2

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FIG. 3

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d_{n-1} → **Register** → d_n —410

400
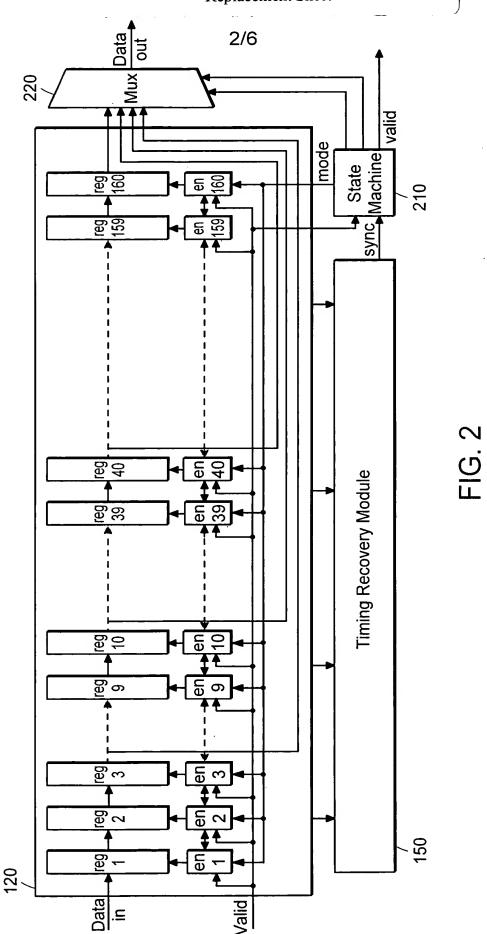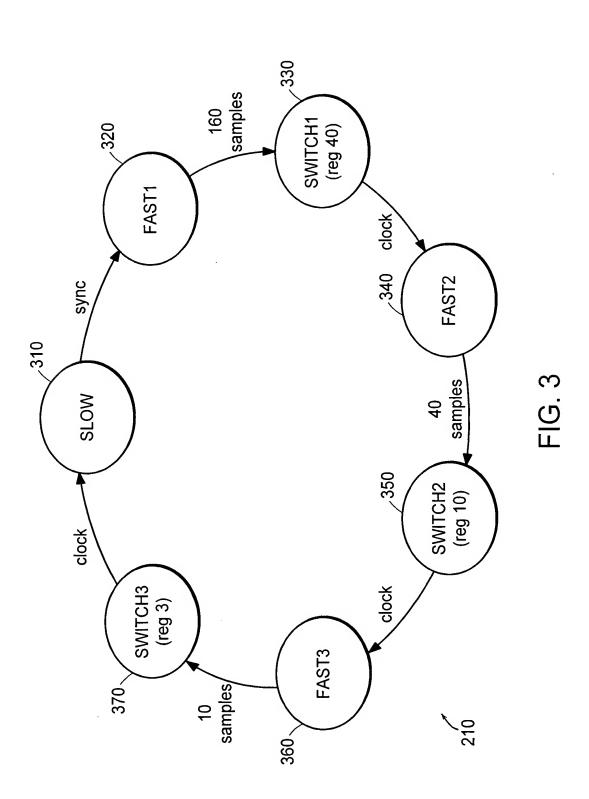
enable

v_{n-1} → **Enable Logic** → v_n —420

valid →

mode →

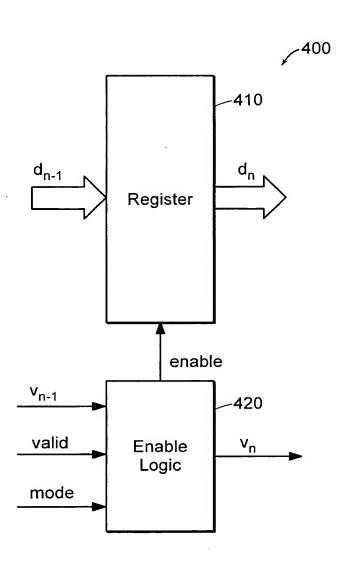# FIG. 4

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Title: "Method and System For Dynamically..."
Inventors: Maneesh Soni, *et al.*
Replacement Sheet

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FIG. 5

Mode	Clock Cycle	Valid Signal (Incoming Sample at Delay Chain Input)	REGISTERS																	
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
SLOW mode	1		+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	2	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	3		+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	4			+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	5				+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	6	+	+			+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	7		+				+	+	+	+	+	+	+	+	+	+	+	+	+	+
	8		+					+	+	+	+	+	+	+	+	+	+	+	+	+
	9		+						+	+	+	+	+	+	+	+	+	+	+	+
FAST mode	10	+	+							+	+	+	+	+	+	+	+	+	+	+
	11		+	+							+	+	+	+	+	+	+	+	+	+
	12		+	+								+	+	+	+	+	+	+	+	+
	13		+	+									+	+	+	+	+	+	+	+
	14	+	+	+										+	+	+	+	+	+	+
	15		+	+	+										+	+	+	+	+	+
	16		+	+	+											+	+	+	+	+
	17		+	+	+												+	+	+	+
	18	+	+	+	+													+	+	+
	19		+	+	+	+														+	+
	20		+	+	+	+															+

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SLOW mode
(*mode* = 0)
READY state
(*state* = 0)

<u>610</u>

sync = 1

FAST mode
(*mode* = 1)
READY state
(*state* = 0)

<u>620</u>

sync = 0

$V_{n-1} = 0$

FAST mode
(*mode* = 1)
NOT READY state
(*state* = 1)

<u>630</u>

FIG. 6